Amendments to the Claims:

Claims 1 to 22 (Canceled)

23. (New) A method of extending a dynamic range for processing signals from an imaging device, comprising:

setting a gain value that determines a range of analog-to-digital converter (ADC) output values for a corresponding range of variable gain amplifier (VGA) input values; and

in response to one of the VGA input values reaching a trip point, which indicates that an ADC output value is out of the range, decreasing the gain value to a next lower gain value and reducing the one of the ADC output values to a lower ADC output value that corresponds to the next lower gain value and the one of the VGA inputs.

24. (New) The method according to Claim 23, further comprising:

setting the trip point to a value slightly less than an ideal trip point value so that the gain value is switched before the ADC output value reaches a full scale value and avoids saturation of the ADC output value.

25. (New) The method according to Claim 24, wherein setting the trip point to a value slightly less than an ideal trip point value further comprises:

utilizing an offset to set the trip point to the value slightly less than the ideal trip point value.

26. The method according to Claim 23, wherein decreasing the gain value to a next lower gain value further comprises:

decreasing the gain value to the next lower gain value which is lower by a factor of two.

27. The method according to Claim 26, wherein reducing the one of the ADC output values to a lower ADC output value that corresponds to the next lower gain value and the one of the VGA inputs further comprises:

decreasing the one of the ADC output values to the lower ADC output value which is lower by a factor of two.

28. The method according to Claim 27, further comprising:

increasing a corresponding range of variable gain amplifier (VGA) input values by a factor of two.

29. The method according to Claim 23 wherein setting a gain value further comprises:

setting a number of gain values that correspond to respective ranges of analog-to-digital converter (ADC) output values for corresponding ranges of variable gain amplifier (VGA) input values.

30. A dynamic range extension signal processing circuit, comprising:

a logic circuitry for extending a dynamic range for processing signals from an imaging device;

an analog-to-digital converter coupled to an input of the logic circuitry; and

a variable gain amplifier coupled to an output of the logic circuitry;

wherein a gain value is set which determines a range of analog-to-digital converter (ADC) output values of the analog-to-digital converter for a corresponding range of variable gain amplifier (VGA) input values of the variable gain amplifier; and

in response to one of the VGA input values reaching a trip point, which indicates that an ADC output value is out of the range, the logic circuitry decreases the gain value to a next lower gain value and reduces the one of the ADC output values to a lower ADC output value that corresponds to the next lower gain value and the one of the VGA inputs.

31. (New) The dynamic range extension signal processing circuit according to Claim 30, wherein:

the trip point for the analog-to-digital converter is set to a value slightly less than an ideal trip point value so that the logic circuitry switches the gain value before the

ADC output value reaches a full scale value and avoids saturation of the ADC output value.

32. (New) The dynamic range extension signal processing circuit according to Claim 31, further comprising a calibration system coupled to the variable gain amplifier wherein the calibration system provides an offset to set the trip point to the value slightly less than the ideal trip point value.

33. The dynamic range extension signal processing circuit according to Claim 30, wherein the logic circuitry decreases the gain value to the next lower gain value which is lower by a factor of two.

34. The dynamic range extension signal processing circuit according to Claim 33, wherein the one of the ADC output values of the analog-to-digital converter is decreased by a factor of two.

35. The dynamic range extension signal processing circuit according to Claim 34, wherein a corresponding range of variable gain amplifier (VGA) input values for the variable gain amplifier is increased by a factor of two.

36. The dynamic range extension signal processing circuit according to Claim 30 wherein a number of gain values are set which correspond to respective ranges of analog-to-digital converter (ADC) output values for corresponding ranges of variable gain amplifier (VGA) input values.